CLAIMS

What is claimed is:

1. A selective etch shallow trench isolation barrier integrated circuit comprising:

a transistor adapted to control electrical signal flow;

an intermetal dielectric layer overlaying said transistor, said intermetal layer adapted to insulate said transistor from other layers;

a contact plug inserted in said intermetal layer, said contact plug adapted to conduct electricity; and

a selective etch shallow trench isolation barrier underlying said intermetal dielectric layer, said selective etch shallow trench isolation barrier adapted to withstand etching processes directed toward said intermetal layer and facilitate isolation of said transistor from outside electrical influences of other devices.

2. A selective etch shallow trench isolation barrier integrated circuit of Claim 1 wherein said selective etch shallow trench isolation barrier comprises silicon nitride or oxynitride.

3. A selective etch shallow trench isolation barrier integrated circuit of Claim 1 wherein said intermetal dielectric layer comprises silicon oxide.

4. A selective etch shallow trench isolation barrier integrated circuit of Claim 1 wherein said contact plug is formed by etching a contact hole in said intermetal dielectric layer and stopping on said selective etch shallow trench isolation barrier.

5. A selective etch shallow trench isolation barrier integrated circuit of Claim 1 wherein said selective etch shallow trench isolation barrier comprises selective etch isolation material that etches selective to other materials adjacent to said selective etch isolation material.

6. A selective etch shallow trench isolation barrier integrated circuit of Claim 1 wherein said selective etch shallow trench isolation barrier comprises material with a relatively high dielectric constant.

7. A selective etch shallow trench isolation barrier integrated circuit of Claim 1 wherein said selective etch shallow trench isolation barrier is adapted to isolate electrically floating devices included in said selective etch shallow trench isolation barrier integrated circuit.

8. A selective etch shallow trench isolation barrier integrated circuit of Claim 1 wherein said selective etch shallow trench isolation barrier has rounded edges.

9. A selective etch shallow trench isolation barrier integrated circuit of Claim 1 wherein said selective etch shallow trench isolation barrier has relatively sharp edges.

10. A selective etch shallow trench isolation barrier integrated circuit chip fabrication process comprising the steps of:

forming a shallow trench space in a wafer;

depositing a selective etch isolation material in a shallow trench space of a device layer to form a selective etch shallow trench isolation barrier;

fabricating an intermetal dielectric layer on top of said device layer;

etching a contact hole in said intermetal dielectric layer down to said selective etch shallow trench isolation barrier; and

filling said contact hole with conductive material.

11. The selective etch shallow trench isolation barrier integrated circuit chip fabrication process of Claim 10 in which said etching of said contact hole in said intermetal layer down to said selective etch shallow trench isolation barrier is a single film layer etch step stopping on selective etch isolation material of said the selective etch shallow trench isolation barrier.

12. The selective etch shallow trench isolation barrier integrated circuit chip fabrication process of Claim 11 in which said intermetal dielectric layer

comprises oxide and said single film layer etch step is performed by Ar, CF_4, CHF_3, CO, and/or C_4F_8.

13 The selective etch shallow trench isolation barrier integrated circuit chip fabrication process of Claim 10 wherein said selective etch isolation material etches differently than other material adjacent to said elective selective etch isolation material.

14 The selective etch shallow trench isolation barrier integrated circuit chip fabrication process of Claim 10 wherein said selective etch isolation material includes silicon nitride or oxynitride.

15 The selective etch shallow trench isolation barrier integrated circuit chip fabrication process of Claim 10 further comprising the steps of:

depositing the selective etch isolation material to fill said shallow trench; and

removing excess elective etch isolation material by a chemical mechanical polishing (CMP) process.

16. A selective etch material shallow trench isolation barrier integrated circuit chip fabrication of Claim 10 further comprising the steps of:

pre-cleaning a wafer using high purity, low particle chemicals;

heating said wafer;

exposing said wafer to ultra-pure oxygen in a diffusion furnace under carefully controlled conditions; and

forming a silicon dioxide film of uniform thickness on the surface of the wafer.

17. A selective etch shallow trench isolation barrier integrated circuit chip fabrication process comprising the steps of:

applying layers of oxide and nitride;

creating a resistive mask pattern;

etching a shallow trench space;

depositing a selective etch isolation material in said shallow trench space to form a selective etch shallow trench isolation barrier;

fabricating an intermetal dielectric layer;

etching a contact hole in said intermetal dielectric layer down to said selective etch shallow trench isolation barrier; and

filling said contact hole with conductive material.

18. The selective etch shallow trench isolation barrier integrated circuit chip fabrication process of Claim 17 in which said etching of said contact hole in said intermetal dielectric layer down to said selective etch shallow trench isolation barrier is a single film layer etch step stopping on selective etch isolation material of said the selective etch shallow trench isolation barrier.

19 The selective etch shallow trench isolation barrier integrated circuit chip fabrication process of Claim 17 wherein said selective etch isolation material etches differently than other material adjacent to said elective selective etch isolation material.

20 The selective etch shallow trench isolation barrier integrated circuit chip fabrication process of Claim 17 wherein said selective etch isolation material includes silicon nitride or oxynitride.